**Amendments to the Drawings:**

Two replacement sheets containing drawing amendments are attached hereto. Please substitute replacement sheets for figure 4-6 in place of the originally filed sheets. No new matter has been added; five changes are made:

(i) In FIG. 4, the reference numeral of the ramp generator has been corrected to read "410," as described in paragraph [0040] of the specification. The ramp generator was originally incorrectly labeled "420," the same numeral as assigned to the synchronizer.

(ii) In FIG. 4, the formatting of the text "PHASE COMPENSATOR" has also been corrected.

(iii) In FIG. 4, the reference numeral "451" has been added to the input of digital low pass filter 460, as supported by paragraph [0045]:

> ". . .. The same signed binary number becomes used as a digital unfiltered VCO correction signal and is sent to multiple conductor port 451. Signed binary number on port 451 is fed to digital LPF (low pass filter) 460 which, precisely because it is digital, may have a long time constant without the use of expensive analog components. Also, since the digital LPF 460 performs essentially a smoothing operation, it may usefully have an output precision considerably greater than the input 451. In one exemplary embodiment, the signed binary number input to the digital LPF input 451 is 4 bits wide (limited primarily by the resolution of the comparator set) and the LPF output 461 is 16 bits of resolution. Greater resolution than that provided by a 16 bit output from the digital LPF 460 may be required for some applications. At the desired operating point of equal or correctly related MRO and VCO frequencies, the correction signal presented on port 451 will be zero. . . ." (Specification, ¶ [0045])

(iv) In FIG. 4, the reference numeral of the over sampled modulator has been corrected to read "470" as described in paragraphs [0046] and [0047]. The over sampled modulator was originally incorrectly labeled "370."

(v) In FIG. 6, the incorrect reference numerals "311" have been changed to "411." The specification does not contain a reference numeral "311."

Attachment: 2 replacement sheets

## REMARKS

Reconsideration and allowance are respectfully requested.

Before entry of this amendment, claims 1-15 were pending. In the Office Action, claims 1-3, 8-11 and 14-15 were rejected, and claims 4-7 and 12-13 were objected to. In the present amendment, claims 1, 4 and 12 are amended, and claims 16-20 are added. After entry of the amendment, claims 1-20 are pending.

### I. Claims 4-7 and 12-13

Claims 4-7 and 12-13 are objected to as being dependent upon rejected base claims, but would be allowable if rewritten in independent form. (See Office Action, p. 5, lines 13-15.) Applicant amends these claims to include all of the limitations of the base claim and any intervening claims. Withdrawal of the objection to claims 4-7 and 12-13 is respectfully requested.

### II. Claims 1-2 and 11

Claims 1-2 and 11 are rejected under 35 U.S.C. § 102(e) as being anticipated by Mergard et al. (USP 6,401,156) (Office Action, p. 2, lines 20-21). Applicant respectfully disagrees and traverses the § 102(e) rejection.

#### A. Independent claim 1

Anticipation under § 102 requires the presence in a single prior art reference that discloses all of the elements of a claimed invention arranged as in the claim. Sandt Tech., Ltd. v. Resco Metal & Plastics Corp., 264 F.3d 1344, 1350 (Fed.Cir. 2001). "To serve as an anticipation when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268 (Fed. Cir. 1991)"

Metabolite Labs., Inc. v. Lab. Corp. of Am. Holdings, 370 F.3d 1354, 1367 (Fed. Cir. 2004) (emphasis added).

Mergard does not form the basis for a valid rejection under § 102(e) because Mergard does not disclose all of the limitations of claim 1. Claim 1 recites a "crystal oscillator circuit outputting a first clock signal . . ., a processor having a clock input lead; and a clock multiplier circuit having an input lead and an output lead, the clock multiplier circuit receiving the first clock signal from the crystal oscillator circuit and generating therefrom a second clock signal, . . . wherein the second clock signal is supplied to the clock input lead of the processor." Mergard discloses neither a clock multiplier circuit nor how such a circuit would be connected within the microcontroller of Mergard.

The Examiner does not state that Mergard discloses a clock multiplier circuit that receives a signal from the crystal oscillator circuit and supplies a signal with a multiplied frequency to the processor. Instead, the Examiner states that "the circuit of Mergard et al. inherently comprises a clock multiplier circuit, which uses a low frequency clock signal of the oscillator circuit for multiplying that frequency for providing a high frequency clock signal for other circuits such as the processor" (Office Action, p. 3, lines 4-8) (emphasis added).

The Examiner's inherency argument is unsubstantiated because the Examiner has cited no extrinsic evidence. Moreover, under the principles of inherency, only if the structure disclosed in Mergard necessarily includes the limitations claim 1, including a clock multiplier circuit, is claim 1 anticipated. The Examiner has not, however, even asserted that the clock signal of Mergard is necessarily multiplied and provided to the processor. For example, the microcontroller of Mergard could be used with a fast clock signal that is divided and provided to other circuits. The processor in Mergard need not necessarily receive a multiplied clock signal. Therefore, the Examiner has not established a *prima facie* case of anticipation under § 102(e) based on inherency.

In addition, claim 1 recites, "a terminal; a crystal oscillator circuit coupled to the terminal . . .." Mergard does not disclose a crystal oscillator circuit on a

microcontroller integrated circuit that is coupled to a terminal of the microcontroller integrated circuit. Mergard does not disclose the structure of clock 124. Mergard does not disclose whether clock 124 includes a clock circuit coupled to a terminal on a microcontroller or whether clock 124 includes a crystal oscillator and an associated clock circuit that are both external to the microcontroller. Thus, Mergard does not form the basis for a valid rejection under § 102(e) because Mergard does not disclose all of the limitations of claim 1.

Reconsideration of the § 102(e) rejection and allowance of claim 1 are requested.

B. Dependent claims 2 and 11

Claim 11 recites that the second clock signal generated by the crystal oscillator circuit can be output onto a second terminal of the microcontroller integrated circuit. Mergard does not disclose a crystal oscillator circuit that outputs a clock signal onto a terminal of the microcontroller of Mergard. Because Mergard does not disclose all of the limitations of claim 11, Mergard does not form the basis for a valid rejection under § 102(e).

Claims 2 and 11 depend from claim 1. In addition to the reasons explained above, dependent claims 2 and 11 are allowable for at least the same reasons for which claim 1 is allowable. Reconsideration of the § 102(e) rejection and allowance of claims 2 and 11 are requested.

III. Rejection of claims 3 and 8-10

Claims 3 and 8-10 are rejected under 35 U.S.C. §103(a) as being unpatentable over Mergard in view of Ferraiolo et al. (US Patent No. 5,757,238) (Office Action, p. 3, lines 18-19). To established a *prima facie* case of obviousness, the Examiner must demonstrate three criteria. The MPEP § 2142 states:

> "To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the reference (or references when combined) must teach or suggest all the claimed limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure . . .. 'To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.' Ex parte Clapp, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985)." MPEP § 2142 (emphasis added).

A. Dependent claim 3

Claim 3 recites "wherein the clock multiplier circuit includes a frequency locked loop, the frequency locked loop including a digital filter." The Examiner states,

> ". . . Mergard et al. does not discloses details of the clock multiplier circuit . . .. Ferraiolo et al. teaches in Fig. 2 a clock multiplier circuit . . .. Therefore, it would have been obvious to one of ordinary skill in the art to implement the clock multiplier circuit taught by Ferraiolo et al. with the prior art (Fig. 2 of Mergard et al.) in order to quickly achieve phase lock at the different operating frequency for the circuit" (Office Action, p. 3. line 21—p. 5, line 5).

The combination of Mergard and Ferraiolo does not form the basis for a valid rejection under § 103(a) for two reasons. First, the references when combined do not teach or suggest all of the claim elements. Second, there is no suggestion or motivation in Ferraiolo to combine Ferraiolo with Mergard. Nor is there any suggestion or motivation in Mergard to combine Mergard with Ferraiolo.

(i) all of claim elements are not taught or suggested.

Neither Mergard nor Ferraiolo teaches or suggests an integrated circuit comprising a clock multiplier circuit that receives a signal from the crystal oscillator circuit and supplies a signal with a multiplied frequency to a processor. The Examiner admits that Mergard does not disclose a clock multiplier circuit. Because the microcontroller of Mergard need not necessarily include a clock multiplier circuit, the conclusion of the Examiner that the circuit of Mergard inherently comprises a clock multiplier circuit is improper. Moreover, Ferraiolo does not teach a clock multiplier circuit that receives a signal from a crystal oscillator circuit and supplies a signal with a multiplied frequency to a processor.

In addition, neither Mergard nor Ferraiolo teaches or suggests a frequency locked loop. Instead, Ferraiolo discloses a phase-locked loop (200). Moreover, Ferraiolo does not disclose using the PLL (200) as a clock multiplier circuit in an integrated circuit that also comprises a crystal oscillator circuit and a processor.

(ii) no suggestion or motivation to combine.

The Examiner points to no suggestion or motivation in Mergard to combine the teachings of Mergard with the teachings of Ferraiolo. There is no suggestion in Mergard to modify the teachings of Mergard with the PLL of Ferraiolo.

The Examiner states that one of ordinary skill in the art would have been motivated to combine the PLL of Ferraiolo with the circuit of FIG. 2 of Mergard "in order to quickly achieve phase lock at the different operating frequency for the circuit" (Office Action, p. 4, lines 4-5). But there is no suggestion in Ferraiolo to incorporate the teachings of Ferraiolo into the microcontroller of Mergard. Ferraiolo does not mention a processor or a microcontroller. In addition, Mergard does not disclose that achieving a quick phase lock is important. In fact, Mergard does not disclose that clock 124 includes a PLL or that clock 124 performs phase locking. These are not considerations in Mergard. Thus, it would not have been obvious to incorporate the PLL of Ferraiolo into an undisclosed clock multiplier circuit or even into clock 124 of Mergard.

Because the combination of Mergard and Ferraiolo does not disclose all of the elements of claim 3, and furthermore because there is no suggestion or motivation to combine Mergard and Ferraiolo even if all of the elements were present, Mergard and Ferraiolo do not form the basis for a valid rejection under § 103(a). In addition, claim 3 depends from claim 1 and is allowable for at least the same reasons for which claim 1 is allowable. Reconsideration of the § 103(a) rejection and allowance of claim 3 is requested.

B. Dependent claims 8-10

Claims 8-10 depend from claim 1 and are allowable for at least the same reasons for which claim 1 is allowable. The rejection of claims 8-10 should therefore be withdrawn. Reconsideration and allowance is requested.

IV. Rejection of claim 14

Claim 14 is rejected under 35 U.S.C. §103(a) as being unpatentable over Mergard (Office Action, p. 4, line 7). Claim 14 recites, "wherein the first frequency is less than 5 megahertz, and wherein the second frequency is greater than 100 megahertz."

Mergard does not form the basis for a valid rejection under § 103(a) because Mergard does not disclose all of the limitations of claim 14. Mergard discloses a clock 124 and not a clock multiplier circuit. The Examiner does not even state that Mergard discloses a clock multiplier circuit that receives a first clock signal of a first frequency and generates a second clock signal having a second frequency. The Examiner incorrectly asserts that the microcontroller of Mergard inherently comprises a clock multiplier circuit. Mergard does not disclose that either the input signal or the output signal of clock 124 has been multiplied. Figure 10 of Mergard shows that clock 124 outputs a signal of 32,768 Hz. Thus, Mergard does not disclose any range of frequency multiplication relating to clock 124. Finally, Mergard does not disclose that clock 124 outputs a signal with a frequency (multiplied or unmultiplied) greater than 100 megahertz.

Mergard does not form the basis for a valid rejection under § 103(a) because Mergard neither discloses a clock multiplier circuit nor even suggests multiplying a frequency less than 5 MHz to yield a frequency greater than 100 MHz. In addition, claim 14 depends from claim 1 and is allowable for at least the same reasons for which claim 1 is allowable. Reconsideration of the § 103(a) rejection and allowance of claim 14 is requested.

V. Rejection of claim 15

Claim 15 is rejected under 35 U.S.C. §103(a) as being unpatentable over Mergard in view of Gulliver et al. (US Patent No. 6,150,889) (Office Action, p. 5, lines 1-2). Claim 15 recites, "wherein which of the first clock signal and the second clock signal is supplied to the input lead of the clock multiplier circuit can be changed by the processor."

The combination of Mergard and Gulliver does not form the basis for a valid rejection under § 103(a) for three reasons. First, the references when combined do not teach or suggest all of the claim elements. Second, there is no reasonable expectation of success by combining the reference teachings. And third, there is no motivation to combine the reference teachings.

Gulliver does not disclose clock signals supplied to the PLL of Gulliver being changed by a processor. Gulliver does not mention a processor or a microcontroller.

Gulliver does not disclose that a backup clock signal selected as the reference signal for the PLL after a failure of the primary clock signal can be changed by a processor. Note that claim 1 recites "wherein the second clock signal is supplied to the clock input lead of the processor." Presumably a processor would fail upon a failure of the primary clock signal and could not thereupon change the clock signal provided to the input lead of a clock multiplier circuit. Thus, there is no reasonable expectation of success.

Mergard does not disclose an input to clock 124. Thus, there is no motivation to change a signal on an undisclosed input to clock 124. Mergard

does not disclose changing to a backup clock signal. There is no suggestion or motivation in Mergard to combine Mergard with a PLL device that regains phase lock in a predictable manner, such as the PLL and reset stage of Gulliver. Moreover, there is no suggestion or motivation in Gulliver to incorporate the PLL and reset stage of Gulliver into clock 124 of Mergard because clock 124 is not a PLL.

Claim 15 depends from claim 1. In addition to the reasons explained above, dependent claim 15 is allowable for at least the same reasons for which claim 1 is allowable. Reconsideration of the § 103(a) rejection and allowance of claim 15 is requested.

VI. New claims 16-20

Applicant is adding new claims 16-20, each of which is supported by the specification and allowable over the cited references. No new matter is added.

VII. Conclusion

In view of the foregoing amendments and remarks, Applicant respectfully submits that the entire application (claims 1-20 are pending) is in condition for allowance. Applicant respectfully requests that a timely Notice of Allowance be issued in this case. The undersigned can be contacted at (925) 621-2121 to discuss any aspect of this application.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

By Darien K. Wallace
Darien K. Wallace

Date of Deposit: June 10, 2005

Respectfully submitted,

Darien K. Wallace

Darien K. Wallace
Attorney for Applicants
Reg. No. 53,736
Customer No. 47,713